Document made available under the Patent Cooperation Treaty (PCT)

International application number: PCT/US2006/015310

International filing date: 21 April 2006 (21.04.2006)

Document type: Certified copy of priority document

Document details: Country/Office: US
Number: 60/673,935
Filing date: 22 April 2005 (22.04.2005)

Date of receipt at the International Bureau: 19 June 2006 (19.06.2006)

Remark: Priority document submitted or transmitted to the International Bureau in compliance with Rule 17.1(a) or (b)

World Intellectual Property Organization (WIPO) - Geneva, Switzerland
Organisation Mondiale de la Propriété Intellectuelle (OMPI) - Genève, Suisse

1477589

THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

June 08, 2006

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THE UNITED STATES PATENT AND TRADEMARK OFFICE OF THOSE PAPERS OF THE BELOW IDENTIFIED PATENT APPLICATION THAT MET THE REQUIREMENTS TO BE GRANTED A FILING DATE.

APPLICATION NUMBER: *60/673,935*
FILING DATE: *April 22, 2005*
RELATED PCT APPLICATION NUMBER: *PCT/US06/15310*

THE COUNTRY CODE AND NUMBER OF YOUR PRIORITY APPLICATION, TO BE USED FOR FILING ABROAD UNDER THE PARIS CONVENTION, IS *US60/673,935*

UNITED STATES PATENT AND TRADEMARK OFFICE · DEPARTMENT OF COMMERCE

Certified by

Jon W. Dudas

Under Secretary of Commerce
for Intellectual Property
and Director of the United States
Patent and Trademark Office

PROVISIONAL PATENT APPLICATION COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 C.F.R. §1.53(c).

Express Mail Label No.: EV 553432430 US	Attorney Docket No.: 681443-1US

INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Samuel	Anderson	Tempe, Arizona

☐ Additional inventors are being named on ____ separately numbered sheets attached hereto

TITLE OF INVENTION (500 characters maximum)

SUPERJUNCTION DEVICE HAVING OXIDE LINED TRENCHES AND METHOD FOR MANUFACTURING A SUPERJUNCTION DEVICE HAVING OXIDE LINED TRENCHES

CORRESPONDENCE ADDRESS

Customer No.: 000570
AKIN GUMP STRAUSS HAUER & FELD LLP
One Commerce Square
2005 Market Street, Suite 2200
Philadelphia, PA 19103
Telephone: 215-965-1200
Facsimile: 215-965-1210

PLACE BAR CODE LABEL HERE

ENCLOSED APPLICATION PARTS (*check all that apply*)

☒ Specification - *Number of Pages:* 22
☒ Drawing(s) - *Number of Sheets:* 16
☐ Application Data Sheet
☐ CD(s), *Number:*
☐ Other (specify) _____

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

☐ Applicant(s) claim Small Entity Status under 37 C.F.R. §1.27 as:
☐ an Independent Inventor, or ☐ a Small Business Concern, or ☐ a Non-Profit Organization.
☒ A check in the amount of $200.^{00}$ under 37 CFR §1.16(k) (Fee Code 1005) is enclosed herewith.
☒ The Commissioner is hereby authorized to charge or credit Deposit Account No. 50-1017 as indicated below.
☐ Provisional Application Filing Fee in the amount of $200.^{00}$ under 37 CFR §116(k) (Fee Code 1005).
☒ Any deficiencies or overpayments in the above-calculated fee.
☒ Any additional fees required under 37 CFR §1.16 or §1.17.

The invention was made by an agency of the United States Government or under a contract with an agency of the U.S. Government.
☒ No.
☐ Yes, the name of the U.S. Government agency and the Government contract number are:

April 22, 2005
Date

Respectfully submitted,

John D. Simmons

John D. Simmons
Reg. No. 52,225
Akin Gump Strauss Hauer & Feld LLP
One Commerce Square
2005 Market Street, Suite 2200
Philadelphia, PA 19103
Direct Dial: 215-965-1268
E-mail: jsimmons@akingump.com

7390448

Equivalent to PTO/SB/16

TITLE OF THE INVENTION

Superjunction Device having Oxide Lined Trenches and
Method for Manufacturing a Superjunction Device
having Oxide Lined Trenches

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device and a method for manufacturing a semiconductor device, and more particularly, to a superjunction device having oxide lined trenches and a method for manufacturing a superjunction device having oxide lined trenches.

Since the invention of superjunction devices by Dr. Xingbi Chen, as disclosed in U.S. Patent 5,216,275, there have been many attempts to expand and improve on the superjunction effect of his invention. U.S. Patent Nos. 6,410,958, 6,300,171 and 6,307,246 are examples of such efforts and are incorporated herein by reference.

U.S. Patent No. 6,410,958 ("Usui, *et al.*") relates to an edge termination structure and a drift region for a semiconductor component. A semiconductor body of the one conductivity type has an edge area with a plurality of regions of the other conductivity type embedded in at least two mutually different planes. Underneath the active zone of the semiconductor component, the drift regions are connected using the underlying substrate.

U.S. Patent No. 6,307,246 ("Nitta, *et al.*") discloses a semiconductor component having a high-voltage sustaining edge structure in which a multiplicity of parallel-connected individual components are disposed in a multiplicity of cells of a cell array. In an edge region, the semiconductor component has cells with shaded source zone regions. During commutation of the power semiconductor component, the shaded source zone regions suppress the switching "on" of a parasitic bipolar transistor caused by the disproportionately large reverse flow current density. Moreover, an edge structure having shaded source zone regions can be produced very easily in technological terms that are discussed in the Nitta, *et al.* patent. It clarifies the effects of parameters and enables the mass production of a superjunction semiconductor device which has a drift layer composed of a parallel PN layer that conducts electricity in the "on" state and is

depleted in the "off" state. The net quantity of active impurities in the N-type drift regions is within the range of 100% to 150% of the net quantity of active impurities in the P-type partition regions. In addition, the width of either one of the N-type drift regions and the P-type partition regions is within the range between 94% and 106% of the width of the other regions.

U.S. Patent No. 6,300,171 ("Frisina") discloses a method for manufacturing an edge structure for a high voltage semiconductor device, including a first step of forming a first semiconductor layer of a first conductivity type, a second step of forming a first mask over the top surface of the first semiconductor layer, a third step of removing portions of the first mask in order to form at least one opening in it, a fourth step of introducing dopant of a second conductivity type in the first semiconductor layer through the at least one opening, a fifth step of completely removing the first mask and of forming a second semiconductor layer of the first conductivity type over the first semiconductor layer, a sixth step of diffusing the dopant implanted in the first semiconductor layer in order to form a doped region of the second conductivity type in the first and second semiconductor layers. The second step up to the sixth step are repeated at least one time in order to form a final edge structure including a number of superimposed semiconductor layers of the first conductivity type and at least two columns of doped regions of the second conductivity type, the columns being inserted in the number of superimposed semiconductor layers and formed by superimposition of the doped regions subsequently implanted through the mask openings, the columns near the high voltage semiconductor device being deeper than the columns farther from the high voltage semiconductor device.

It is desirable to provide a superjunction device having an oxide liner and a method for manufacturing a superjunction device having oxide lined trenches. It is also desirable to provide a method for manufacturing such a superjunction device utilizing micro-electro-mechanical systems (MEMS) technology to machine the semiconductor substrate during processing.

BRIEF SUMMARY OF THE INVENTION

Briefly stated, the present invention comprises a method of manufacturing a semiconductor device. To begin the process, a semiconductor substrate having first and second main surfaces opposite to each other is provided. The semiconductor substrate has a heavily doped region of a first conductivity type at the second main surface and has a lightly doped region of the first conductivity type at the first main surface. A plurality of trenches and a plurality of mesas are provided in the semiconductor substrate with each mesa having an adjoining trench and a first extending portion extending from the first main surface toward the heavily doped region to a first depth position. At least one mesa has a first sidewall surface and a second sidewall surface. Each of the plurality of trenches has a bottom. The method includes implanting a dopant of a second conductivity type into the first sidewall surface of the at least one mesa to form a first doped region of the second conductivity type. The method also includes implanting a dopant of a second conductivity type into the second sidewall surface of the at least one mesa to form a third doped region of the second conductivity type. The method includes implanting a dopant of the first conductivity type into a first sidewall surface of the at least one mesa to provide a second doped region of the first conductivity type at the first sidewall, and implanting the dopant of the first conductivity type into the second sidewall of the at least one mesa to provide a fourth doped region of the first conductivity type at the second sidewall. The dopants are then diffused into the at least one mesa to provide a first doped region of the second conductivity type at the second sidewall surface. At least the trenches adjacent to the at least one mesa are then lined with an oxide material and are then filled with one of a semi-insulating material and an insulating material.

In another aspect, the present invention comprises a method of manufacturing a semiconductor device. To begin the process, a semiconductor substrate having first and second main surfaces opposite to each other is provided. The semiconductor substrate has a heavily doped region of a first conductivity type at the second main surface and has a lightly doped region of the first conductivity type at the first main surface. A plurality of trenches and a plurality of mesas are provided with each mesa having an adjoining trench and a first extending portion extending from the first main surface toward the heavily doped region to a first depth

position. At least one mesa has a first sidewall surface and a second sidewall surface. Each of the plurality of trenches has a bottom. The method includes implanting a dopant of a first conductivity type into the first sidewall surface of the at least one mesa to form a first doped region of the first conductivity type. The method also includes implanting a dopant of the first conductivity type into the second sidewall surface of the at least one mesa to form a second doped region of the first conductivity type. The method includes implanting a dopant of the second conductivity type into a first sidewall surface of the at least one mesa to provide a second doped region of the first conductivity type at the first sidewall, and implanting the dopant of the second conductivity type into the second sidewall of the at least one mesa. The dopants are then diffused into the at least one mesa to provide a first doped region of the second conductivity type at the second sidewall surface. At least the trenches adjacent to the at least one mesa are then lined with an oxide material and are then filled with one of a semi-insulating material and an insulating material.

The present invention also comprises the semiconductors formed by the above methods.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

The file of this provisional patent application contains at least one drawing executed in color. Copies of this patent with color drawings will be provided by the Patent and Trademark Office upon request and payment of the necessary fee.

The foregoing summary, as well as the following detailed description of preferred embodiments of the invention, will be better understood when read in conjunction with the appended drawings. For purposes of illustrating the invention, there are shown in the drawings embodiments which are presently preferred. It should be understood, however, that the invention is not limited to the precise arrangements and instrumentalities shown.

Fig. 1 is a partial sectional elevational view of an N type semiconductor substrate having an oxide liner in accordance with a first preferred embodiment of the present invention;

Fig. 2 is a partial sectional elevational view of an N type semiconductor substrate;

Fig. 3 is a partial sectional elevational view of the semiconductor substrate of Fig. 2 after an etch step, implanting a P conductivity dopant at first and second predetermined angles of implant and diffusing the implanted ions;

Fig. 4 is a partial sectional elevational view of the semiconductor substrate of Fig. 3 after implanting an N conductivity dopant at the first and second predetermined angles of implant and diffusing the implanted ions;

Fig. 5 is a partial sectional elevational view of the semiconductor substrate of Fig. 4 after lining with an oxide material, refilling with a semi-insulative material and planarizing;

Fig. 6 is a partial sectional elevational view of the semiconductor substrate of Fig. 5 showing the device prepared for formation of an active device;

Fig. 7 is a partial sectional elevational view of a cell description of a planar metal-oxide semiconductor field effect transistor (MOSFET) N type structure using a standard planar process in accordance with the first preferred embodiment;

Fig. 8 is a partial sectional elevational view of a cell description of a planar metal-oxide semiconductor field effect transistor (MOSFET) N type structure using a standard planar process in accordance with an alternate of the first preferred embodiment;

Fig. 9 is a partial sectional elevational view of an N type semiconductor substrate having an oxide liner and a buffer layer in accordance with a second preferred embodiment of the present invention;

Fig. 10 is a partial sectional elevational view of an N type semiconductor substrate having an oxide liner in accordance with a third preferred embodiment of the present invention;

Fig. 11 is a partial sectional elevational view of an N type semiconductor substrate;

Fig. 12 is a partial sectional elevational view of the semiconductor substrate of Fig. 11 after an etch step, implanting an N conductivity dopant at first and second predetermined angles of implant and diffusing the implanted ions;

Fig. 13 is a partial sectional elevational view of the semiconductor substrate of Fig. 12 after lining with an oxide material and filling with undoped polysilicon;

Fig. 14 is a partial sectional elevational view of the semiconductor substrate of Fig. 13 after refilling with undoped polysilicon and planarizing;

Fig. 15 is a partial sectional elevational view of the semiconductor substrate of Fig. 14 showing the device prepared for formation of an active device;

Fig. 16 is a partial sectional elevational view of a cell description of a planar metal-oxide semiconductor field effect transistor (MOSFET) N type structure using a standard planar process in accordance with the third preferred embodiment; and

Fig. 17 is a partial sectional elevational view of an N type semiconductor substrate having an oxide liner and a buffer layer in accordance with a fourth preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Certain terminology is used in the following description for convenience only and is not limiting. The words "right", "left", "lower", and "upper" designate directions in the drawing to which reference is made. The words "inwardly" and "outwardly" refer direction toward and away from, respectively, the geometric center of the object described and designated parts thereof. The terminology includes the words above specifically mentioned, derivatives thereof and words of similar import. Additionally, the word "a", as used in the claims and in the corresponding portions of the specification, means "at least one."

Figs. 1-6 generally show a process for manufacturing an N type structure in accordance with a first preferred embodiment of the present invention.

Referring to Fig. 2, there is shown a partial elevational view of a semiconductor wafer that includes an N^{++} substrate 3 and an N epitaxial layer 5. As used herein, reference to conductivity will be limited to the embodiment described. However, those skilled in the art know that P-type conductivity can be switched with N-type conductivity and the device would

still be functionally correct (i.e., a first or a second conductivity type). Therefore, where used herein, the reference to N or P can also mean that either N and P or P and N can be substituted. Metal oxide semiconductor field effect transistor (MOSFET)-gated devices such as insulated gate bipolar transistors (IGBTs) can be fabricated in an epitaxial wafer with an N-type epitaxial layer over a P^+ substrate (or visa versa).

Fig. 1 demonstrates the steps necessary to form a partially manufactured superjunction device in accordance with the present invention.

Referring to Fig. 3, using techniques known in the art, the epitaxial layer 5 is etched to touch or to approach an interface between the substrate 3 and the epitaxial layer 5. The etch process creates trenches 9 and mesas 11. The mesas 11, which are "device mesas," will be used to form the voltage sustaining layer for each transistor or active device cell manufactured by the process. The mesas 11 are referred to as device mesas because the mesas 11 are in an active region, as opposed to a surrounding termination or edge termination region. The active region is the area on which semiconductor devices will be formed, and the termination region is an area which provides insulation between cells of active devices.

The separation of the mesas 11, i.e., the width A of the trenches 9, and the depth B of the trenches 9 is used to determine an implantation angle Φ, Φ' (i.e., a first or second angle of implant Φ, Φ') of ion implants that are to be performed and discussed later. For the same reason, the width A between the mesas 11 and the edge termination region is also approximately the same distance. Though not shown clearly, in some embodiments the trenches 9 are preferably slightly wider at their tops by about 1%-10% than at their bottoms to facilitate the trench fill process when the trenches 9, for example, are to be filled with grown oxide. Consequently, the mesas 11, in embodiments with trenches 9 having wider tops, have a first sidewall surface with a predetermined inclination maintained relative to the first main surface and a second sidewall surface with a predetermined inclination maintained relative to the first main surface. The inclination of the first sidewall surface is about the same as the inclination of the second sidewall surface depending on tolerances of the etching process.

In other embodiments, it is desirable to have the sidewalls of the mesas 11 as vertical as possible (i.e., 0° inclination angle). While the first trenches 9 extend from the first main surface

of the epitaxial layer 5 toward the substrate (heavily doped region) 3 to the first depth position by depth B, the first trenches 9 do not necessarily extend all the way to the substrate (heavily doped region) 3.

Preferably, the etching is performed by utilizing micro-electro-mechanical systems (MEMS) technology to machine the semiconductor substrate during processing. MEMS technology permits deeper trenches 9 with much straighter sidewalls. Utilizing MEMS technology, trenches 9 can be formed having depths B of about 40 to 100 micrometers or microns (μm) or even deeper. Furthermore, forming deeper trenches 9 that have straighter sidewalls than conventionally etched or formed trenches 9, in addition to other steps in the process, results in a final superjunction device with enhanced avalanche breakdown voltage (V_b) characteristics as compared to conventional semiconductor-transistor devices (i.e., the avalanche breakdown voltage (V_b) can be increased to about 200 to 1200 Volts or more). MEMS technology (i.e., machining for trenching, etching, planarizing and the like) can be utilized with any of the embodiments of the present invention.

The sidewalls of each trench 9 may be smoothed, if needed, using one or more of the following process steps: (i) an isotropic plasma etch may be used to remove a thin layer of silicon (typically 100-1000 Angstroms) from the trench surfaces or (ii) a sacrificial silicon dioxide layer may be grown on the surfaces of the trench and then removed using an etch such as a buffered oxide etch or a diluted hydrofluoric (HF) acid etch. The use of either or both of these techniques can produce smooth trench surfaces with rounded corners while removing residual stress and unwanted contaminates. However, in the embodiments where it is desirable to have vertical sidewalls and square corners, an anisotropic etch process will be used instead of the isotropic etch process discussed above. Anisotropic etching, in contrast to isotropic etching, generally means different etch rates in different directions in the material being etched.

Many geometrical arrangements of trenches 9 and mesas 11 (i.e., in plan view) are also contemplated without departing from the invention.

Referring to Fig. 3, at a slight angel Φ (i.e., a first predetermined angle of implant Φ), without benefits of a masking step, the mesas 11 are implanted by a P dopant such as boron (B) (i.e., a dopant having a second conductivity or P conductivity) on one side at a high energy level

in the range of about 40 Kilo-electron-volts (KeV) to several Mega-eV. Preferably, the energy level is in the range of about 200 KeV to 1 MeV, but it should be recognized that the energy level should be selected to sufficiently implant the dopant. The first predetermined angle of implant Φ, as represented by thick arrows, is determined by the width A between the mesas 11 and the depth B of the trenches 9 and can be between about 2° and 12° from vertical and is preferably about 4°. The use of the width A and depth B to determine the first predetermined angle of implant Φ ensures that only the sidewalls of the trenches 9 and not the bottoms of the trenches 9 in the active region are implanted. Consequently, a dopant of the second conductivity type is implanted, at a first predetermined angle of implant Φ, into at least one preselected mesa 11 to form at the sidewall surface of the one trench 9 a first doped region of the second conductivity type having a doping concentration lower than that of the heavily doped region.

The opposite sides of the mesas 11 are implanted with boron B at a second predetermined angle of implant Φ', as represented by thick arrows. Similar to the first predetermined angle of implant Φ, the second predetermined angle of implant Φ' is determined by the width A between the mesas 11 and the depth B of the trenches 9 and can be between about -2° and -12° from vertical and preferably at about -4°. The use of the width A and depth B to determine the second predetermined angle of implant Φ' ensures that only the sidewalls of the trenches 9 and not the bottoms of the trenches 9 in the active region are implanted. Consequently, a dopant of the second conductivity type is implanted, at a second predetermined angle of implant Φ', into at least one preselected mesa 11 to form at the sidewall surface of the one trench 9 a second doped region of the second conductivity type having a doping concentration lower than that of the heavily doped region.

Following implanting the second P type implant (Fig. 3), a drive in step (i.e., a diffusion) is performed at a temperature of up to about 1200° Celsius for up to about 24 hours so that the mesas 11 are converted to P-P columns 22 (Fig. 4). It should be recognized that the temperature and time are selected to sufficiently drive in the implanted dopant.

As shown in Fig. 4, second implant is then performed with an N type dopant such as phosphorous (P) or arsenic (As). The N type implant is performed at the first predetermined angle of implant Φ and at an energy level of about 30 KeV to 1 MeV. Preferably, the energy

level is in the range of about 40 to 300 KeV, but it should be recognized that the energy level should be selected to sufficiently implant the dopant. In Fig. 4, opposite sides of the P-P columns 22 are implanted with the N type dopant at the second predetermined angle of implant Φ', as well.

Following the second N type implant, a drive in step (i.e., diffusion) is performed at a temperature of up to about 1200° Celsius for up to about 24 hours resulting in the P-P pillars 22 being converted to NP-PN columns 27 (Fig. 5) and right side termination N and P region 31 as shown in Fig. 5.

The trenches 9 are then lined or coated with a thin layer of an oxide dielectric material forming an oxide liner 133 on the sides of the NP-PN columns 27 and the bottoms of the trenches 9. The lining of the trenches is performed using a technique known as low pressure (LP) chemical vapor deposition (CVD) Tetraethylorthosilicate (TEOS) or simply "LPTEOS." Alternatively, a spun-on-glass (SOG) technique or any other deposited oxide layer may be used to line the trenches 9 with the oxide liner 133. Preferably, the oxide liner 133 is about 100 Angstroms (Å) to 10,000 Å thick (1 μm = 10,000 Å). The oxide liner 133 reduces charges on the surface of the silicon in the trenches 9 because the oxide will "consume" the charges on the surface of the walls of the trenches 9.

The trenches 9 are then refilled (filled) with a semi-insulating material or doped or undoped polysilicon (poly) 190. The semi-insulating material can be semi-insulating polycrystalline silicon (SIPOS). Preferably, the trenches 9 are refilled with SIPOS 190. The amount of oxygen content in the SIPOS is selectively chosen to be between 2% and 80% to improve the electrical characteristics of the active region. Increasing the amount of oxygen content is desirable for electrical characteristics, but varying the oxygen content also results in altered material properties. Higher oxygen content SIPOS will thermally expand and contract differently than the surrounding silicon which may lead to undesirable fracturing or cracking especially near the interface of differing materials. Accordingly, the oxygen content of the SIPOS is optimally selected to achieve the most desirable electrical characteristics without an undesirable impact on mechanical properties.

Fig. 6 shows that after refill, the device is planarized using chemical mechanical polishing (CMP) or other techniques known in the art. The N/P columns 27 are exposed in order to create the device features for a transistor to be formed thereon. The amount of planarization is about 0.6-3.2 μm. The amount of planarization is chosen so as to sufficiently expose the N/P columns 27, but not to open any internal voids in the fill material 190 that may have occurred during the fill process. Preferably, the planarization is about 1.0-1.5 μm. P type termination rings can then be added in the termination region 31.

Figs. 7 and 8 are partial sectional elevational views of a cell descriptions (i.e., configurations of individual devices or cells of a single-cell or multi-cell chip) of planar metal-oxide semiconductor field effect transistor (MOSFET) N type structures using a standard planar process in accordance with the first preferred embodiment.

Fig. 7 shows an NP-PN mesa device in accordance with the first preferred embodiment having an NP-PN column 27 that is isolated from other neighboring cells by the oxide liner 133 and SIPOS or poly refill 190. The substrate 3 functions as a drain and the NP-PN column 27 is disposed thereon. The device also includes a source region 505. The source region 505 includes a P region 501 in which there are formed N source regions 502. Oxide layers 506 separates a pair of gate poly regions 504 from the N source connectors 502 and the P region 501.

Fig. 8 shows an alternate of the first preferred embodiment with a PN-NP mesa device in which is used in the N type planar MOS structure. The device has a PN-NP column 127 that is isolated from other neighboring cells by the oxide liner 133 and the SIPOS or poly refill 190. The substrate 3 functions as a drain and the PN-NP column 127 is disposed thereon. The device also includes a source region 1505. The source region 1505 includes a P region 1501 in which there is formed N source region 1502. An oxide layer 1506 separates a gate poly region 1504 from the N source connector 1502 and the P region 1501.

Fig. 9 shows a semiconductor device having an oxide liner 133 in accordance with a second preferred embodiment of the present invention. The second preferred embodiment is similar to the first preferred embodiment except that the trenches 9 do not extend all the way to the interface between the epitaxial layer 5 and the N^{++} substrate 3. Instead, there is a buffer layer

on the order of about 1 μm to 25 μm from the bottoms of the trenches 9 to the interface between the epitaxial layer 5 and the N^{++} substrate 3.

The mesas 11 (Fig. 3) and/or columns 27 (Fig. 9) are shown having a width that is wider than mesas of conventional devices and wider than the trenches 9 (Fig. 3), although the preferred embodiments may be suitable for devices with mesas and/or columns that have a width which is the same as or is narrower than conventional mesas and/or columns. The width of the mesas and/or columns should not be construed as limiting.

Figs. 10-15 generally show a process for manufacturing an N type structure in accordance with a third preferred embodiment of the present invention.

Fig. 10 shows the third preferred embodiment of an N type structure that includes NN columns 327 that are separated by a double P (2P) doped polysilicon refill 390. Fig. 10 also shows the steps for forming a semiconductor device in accordance with the third preferred embodiment.

Fig. 11 shows that, similar to the first preferred embodiment, the process begins with an N^{++} substrate 3 having an N type epitaxial layer 5 thereon. An etch formed in N epitaxial layer 5 that approaches the N^{++} substrate 3 to form N mesas 311 that are separated by trenches 309 as shown in Fig. 12. Thereafter, N type dopant is implanted at a first predetermined angle of implant Φ into one side of the mesas 311 and then the other side of the mesas 311 are implanted with the N type dopant at the second predetermined angle of implant Φ'. Following the N type implant, a drive in step (i.e., diffusion) is performed at a temperature of up to about 1200° Celsius for up to about 24 hours resulting in the N mesas 311 (Fig. 13) being converted to N pillars 327 (Fig. 14).

Figs. 13 and 14 show that the trenches 309 are filled with a thin layer of oxide material forming an oxide liner 133 on the sides of the N-N pillars 327 and the bottoms of the trenches 309. The oxide liner 133 is preferably formed by LPCVD TEOS. Preferably, the oxide liner 133 is about 100 Å to 10,000 Å. The trenches 309 are then filled with a thin layer of undoped polysilicon 390 on the sides of the N-N pillars 327 and the bottoms of the trenches 309 over the oxide liner 133. Preferably, the undoped polysilicon layer 365 is about 100 Å to 10,000 Å.

Following the lining of the bottoms of the trenches 309 and the sidewalls of N-N pillars 327, a P type dopant is implanted at the first predetermined angle of implant Φ (similar to Fig. 4) following which the other side of the N-N pillar 327 are implanted with a P type dopant at the second predetermined angle of implant Φ. Thereafter, an undoped polysilicon refill is performed resulting in a 2P poly fill 390 (Fig. 14), and a planarization process is performed. Additionally, a diffusion may optionally be performed before the planarization process is performed. Finally, the device surface can be cleaned and P body implant and cell creation are performed.

Fig. 16 shows a cellular structure of a device in accordance with the third preferred embodiment having an N pillar 327 that is isolated from other neighboring cells by the oxide liner 133 and 2P poly refill 390. The device includes an N-N pillar 327 mounted on the substrate 3, which is a drain, and the active portion of the device is isolated from the other neighboring cells by the oxide liner 133 and 2P poly region 390. The device also includes a source region 305. The source region 305 includes a P region 301 in which there is formed N source region 302. An oxide layer 306 separates a gate poly region 304 from the N source connector 302 and the P region 301.

Fig. 17 shows a semiconductor device having an oxide liner 133 in accordance with a fourth preferred embodiment of the present invention. The fourth preferred embodiment is similar to the third preferred embodiment except that the trenches 309 do not extend all the way to the interface between the epitaxial layer 5 and the N^{++} substrate 3. Instead, there is a buffer layer on the order of about 1 μm to 25 μm from the bottoms of the trenches 309 to the interface between the epitaxial layer 5 and the N^{++} substrate 3.

As mentioned above, the processes are versatile as the N columns and P columns can be exchanged. For the manufacture of P-channel, devices the substrate is P^+ and for an N-channel devices the substrate is N^+. The refill material can be doped or undoped oxide, semi-insulating material (such as SIPOS), doped or undoped polysilicon (poly), nitride or a combination of materials. The different embodiments can be use to make MOSFETs and Schottky diodes and similar devices.

Finally the edge termination regions may include either floating rings or a field plate termination without departing from the invention.

From the foregoing, it can be seen that the present invention is directed to a superjunction device having oxide lined trenches and method for manufacturing a superjunction device having an oxide lined trenches. It will be appreciated by those skilled in the art that changes could be made to the embodiments described above without departing from the broad inventive concept thereof. It is understood, therefore, that this invention is not limited to the particular embodiments disclosed, but it is intended to cover modifications within the spirit and scope of the present invention as defined by the appended claims.

CLAIMS

I claim:

1. A method of manufacturing a semiconductor device comprising:

providing a semiconductor substrate having first and second main surfaces opposite to each other, the semiconductor substrate having a heavily doped region of a first conductivity type at the second main surface and having a lightly doped region of the first conductivity type at the first main surface;

providing in the semiconductor substrate a plurality of trenches and a plurality of mesas with each mesa having an adjoining trench and a first extending portion extending from the first main surface toward the heavily doped region to a first depth position, at least one mesa having a first sidewall surface and a second sidewall surface, each of the plurality of trenches having a bottom;

implanting a dopant of a second conductivity type into the first sidewall surface of the at least one mesa to form a first doped region of the second conductivity type;

implanting a dopant of the second conductivity type into the second sidewall surface of the at least one mesa to form a second doped region of the second conductivity type;

implanting a dopant of the first conductivity type into a first sidewall surface of the at least one mesa to provide a second doped region of the first conductivity type at the first sidewall, and implanting the dopant of the first conductivity type into the second sidewall surface of the at least one mesa to provide a fourth doped region of the first conductivity type at the second sidewall;

diffusing the implanted dopants into the at least one mesa to provide a second doped region of the first conductivity type at the second sidewall surface;

lining at least the trenches adjacent to the at least one mesa with an oxide material; and

filling at least the trenches adjacent to the at least one mesa with one of a semi-insulating material and an insulating material.

2. The method according to claim 1, wherein the oxide lining is formed by one of low pressure (LP) chemical vapor deposition (CVD) Tetraethylorthosilicate (TEOS) and a spun-on-glass (SOG) deposition.

3. The method according to claim 1, further comprising:

forming a layer of undoped polysilicon, after the oxide lining step, over the trench bottoms and the mesas, each including the first and second sidewalls.

4. The method according to claim 1, wherein the step of filling the plurality of trenches with one of a semi-insulating material and an insulating material includes filling the plurality of trenches with at least one of undoped polysilicon, doped polysilicon, doped oxide, undoped oxide, silicon nitride and semi-insulating polycrystalline silicon (SIPOS).

5. The method according to claim 1, wherein the first sidewall surface has a first predetermined inclination maintained relative to the first main surface and the second sidewall surface has a second predetermined inclination maintained relative to the first main surface.

6. The method according to claim 1, wherein the first and second sidewall surfaces are generally perpendicular relative to the first main surface.

7. The method according to claim 1, wherein the plurality of trenches are formed utilizing micro-electro-mechanical systems (MEMS) technology to machine the semiconductor substrate.

8. The method according to claim 1, wherein the implanting of the dopant of a second conductivity type into the first sidewall surface is performed at a first predetermined angle of implant.

9. The method according to claim 1, wherein the implanting of the dopant of a second conductivity type into the second sidewall surface is performed at a second predetermined angle of implant.

10. The method according to claim 1, wherein the implanting of the dopant of the first conductivity type into the first sidewall surface is performed at the first predetermined angle of implant.

11. The method according to claim 1, wherein the implanting of the dopant of the first conductivity type into the second sidewall surface is performed at the second predetermined angle of implant.

12. The method according to claim 1, further comprising:

diffusing the implanted dopants of the second conductivity type into the at least one mesa prior to implanting the dopants of the first conductivity type.

13. A semiconductor formed by the method of claim 1.

14. A method of manufacturing a semiconductor device comprising:

providing a semiconductor substrate having first and second main surfaces opposite to each other, the semiconductor substrate having a heavily doped region of a first conductivity type at the second main surface and having a lightly doped region of the first conductivity type at the first main surface;

providing in the semiconductor substrate a plurality of trenches and a plurality of mesas, with each mesa having an adjoining trench and a first extending portion extending from the first main surface toward the heavily doped region to a first depth position, at least one mesa having a first sidewall surface and a second sidewall surface, each of the plurality of trenches having a bottom;

implanting a dopant of a first conductivity type into the first sidewall surface of the at least one mesa to form a first doped region of the first conductivity type;

implanting a dopant of the first conductivity type into the second sidewall surface of the at least one mesa to form a second doped region of the first conductivity type;

implanting a dopant of the second conductivity type into a first sidewall surface of the at least one mesa to provide a second doped region of the first conductivity type at the first sidewall, implanting the dopant of the second conductivity type into the second sidewall of the at least one mesa;

diffusing the implanted dopants into the at least one mesa to provide a first doped region of the second conductivity type at the second sidewall surface;

lining at least the trenches adjacent to the at least one mesa with an oxide material; and

filling at least the trenches adjacent to the at least one mesa with one of a semi-insulating material and an insulating material.

15. The method according to claim 14, wherein the oxide lining is formed by one of low pressure (LP) chemical vapor deposition (CVD) Tetraethylorthosilicate (TEOS) and a spun-on-glass (SOG) deposition.

16. The method according to claim 14, further comprising:

forming a layer of undoped polysilicon, after the oxide lining step, over the trench bottoms and the mesas, each including the first and second sidewalls.

17. The method according to claim 14, wherein the step of filling the plurality of trenches with one of a semi-insulating material and an insulating material includes filling the

plurality of trenches with at least one of undoped polysilicon, doped polysilicon, doped oxide, undoped oxide, silicon nitride and semi-insulating polycrystalline silicon (SIPOS).

18. The method according to claim 14, wherein the first sidewall surface has a first predetermined inclination maintained relative to the first main surface and the second sidewall surface has a second predetermined inclination maintained relative to the first main surface.

19. The method according to claim 14, wherein the first and second sidewall surfaces are generally perpendicular relative to the first main surface.

20. The method according to claim 14, wherein the plurality of trenches are formed utilizing micro-electro-mechanical systems (MEMS) technology to machine the semiconductor substrate.

21. The method according to claim 14, wherein the implanting of the dopant of a second conductivity type into the first sidewall surface is performed at a first predetermined angle of implant.

22. The method according to claim 14, wherein the implanting of the dopant of a second conductivity type into the second sidewall surface is performed at a second predetermined angle of implant.

23. The method according to claim 14, wherein the implanting of the dopant of the first conductivity type into the first sidewall surface is performed at the first predetermined angle of implant.

24. The method according to claim 14, wherein the implanting of the dopant of the first conductivity type into the second sidewall surface is performed at the second predetermined angle of implant.

25. The method according to claim 14, further comprising:

diffusing the implanted dopants of the second conductivity type into the at least one mesa prior to implanting the dopants of the first conductivity type.

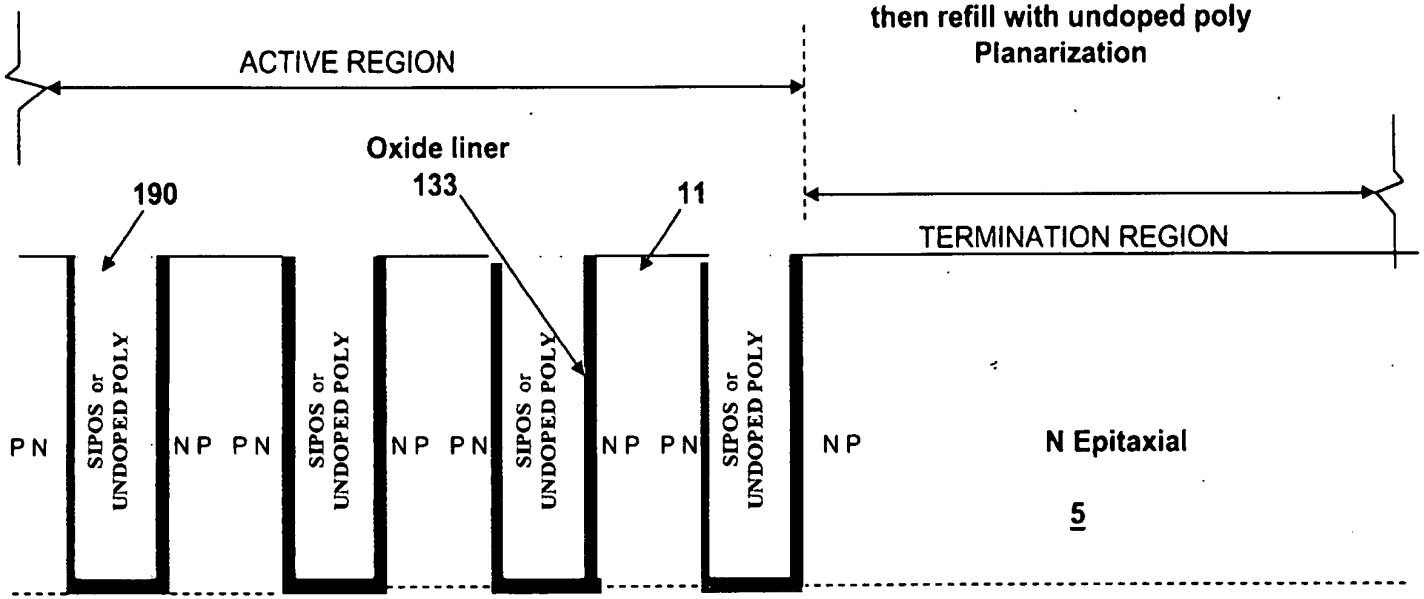
26. A semiconductor formed by the method of claim 14.

ABSTRACT

A method of manufacturing a semiconductor device includes providing semiconductor substrate having trenches and mesas. At least one mesa has first and second sidewalls. The method includes implanting a dopant of a second conductivity into the first sidewall of the at least one mesa, and implanting a dopant of a second conductivity into the second sidewall of the at least one mesa. A dopant of the first conductivity is then implanted into the first sidewall of the at least one mesa, and the dopant of the first conductivity is implanted into the second sidewall of the at least one mesa. The dopants are then diffused into the at least one mesa. At least the trenches adjacent to the at least one mesa are then lined with an oxide material and are then filled with one of a semi-insulating material and an insulating material.

Embodiment 1
N-Type Structure

Trench etch
P implant +4 degree
P implant -4 degree
Diffusion
N implant +4 degree
N implant -4 degree
Diffusion
Trench refill with Oxide liner
(100 Angstroms (Å) to 10,000 Å or 1 micrometer (μm))
then refill with undoped poly
Planarization



Notes: (1) N_column and P_column can be exchanged
(2) For P Channel device, substrate is P+,
(3) For N Channel device, substrate is N+
(4) The Oxide liner is formed by LPCVD TEOS
(5) the fill can be SIPOS (O_2 content from 1% to 99%) or undoped Poly
(6) The method can be used to make N-MOSFET , P-MOSFET and Schottky diode

Fig. 1

Embodiment 1
N-Type Structure

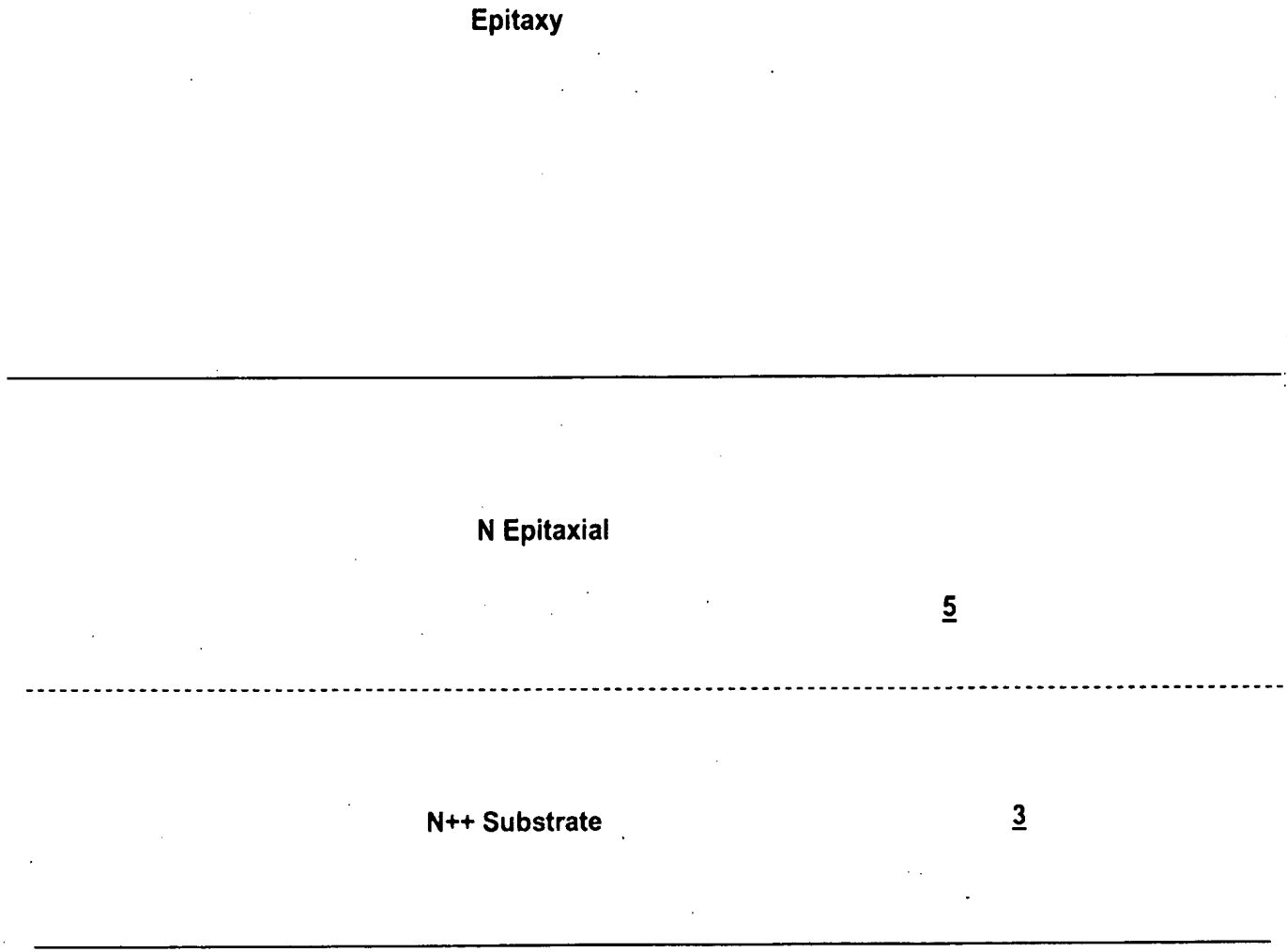


Fig. 2

Embodiment 1
N-Type Structure

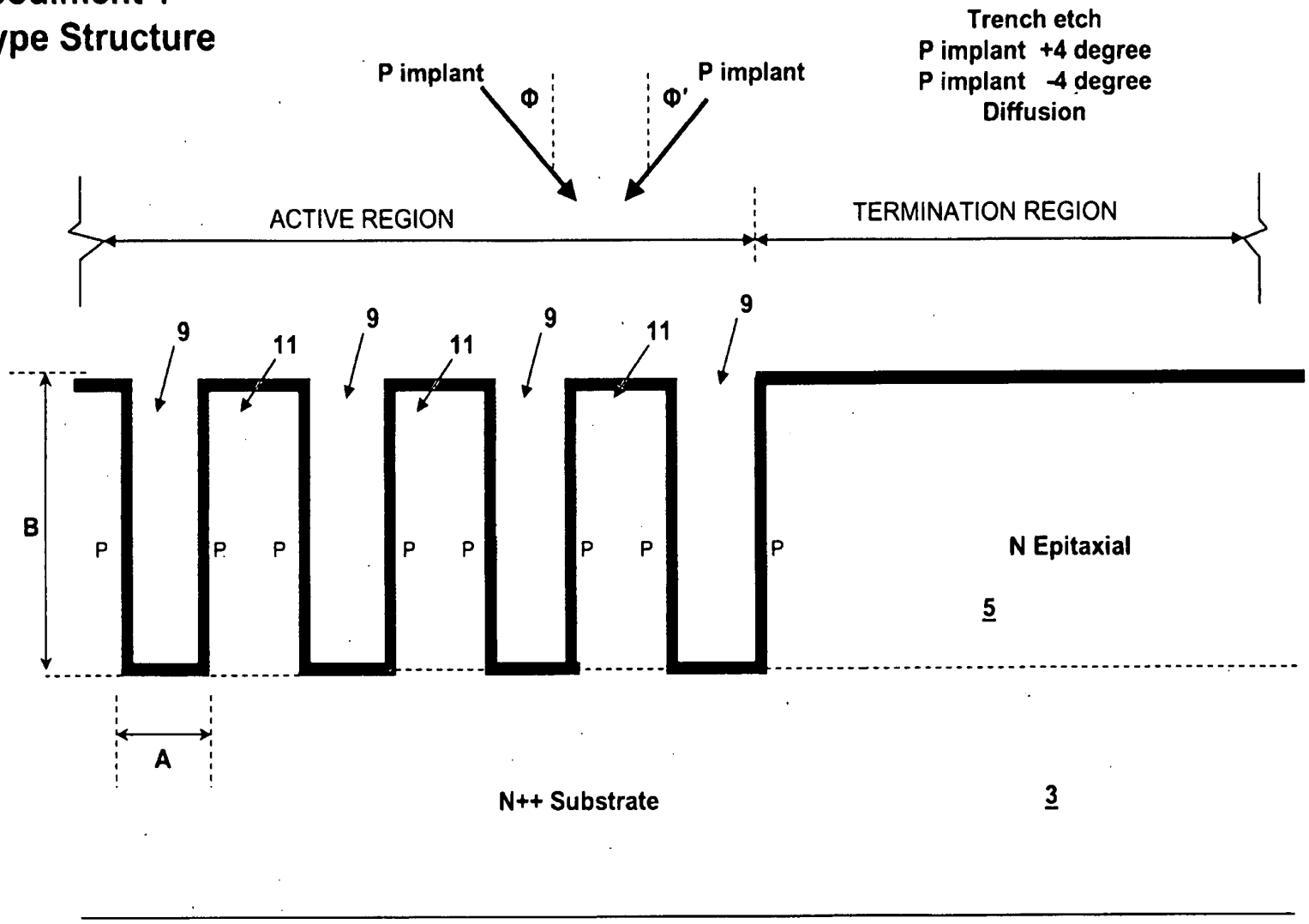
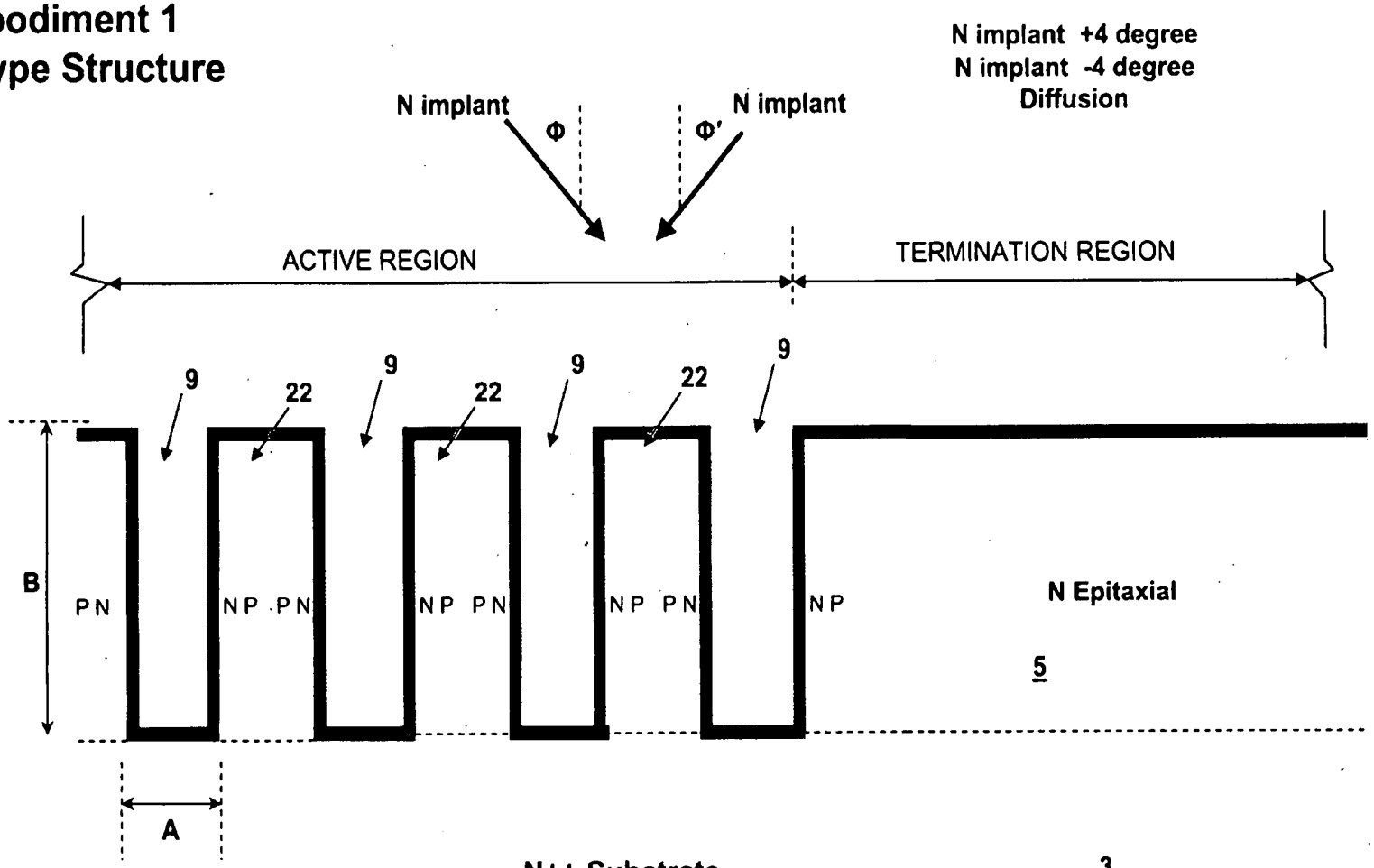


Fig. 3

Embodiment 1
N-Type Structure



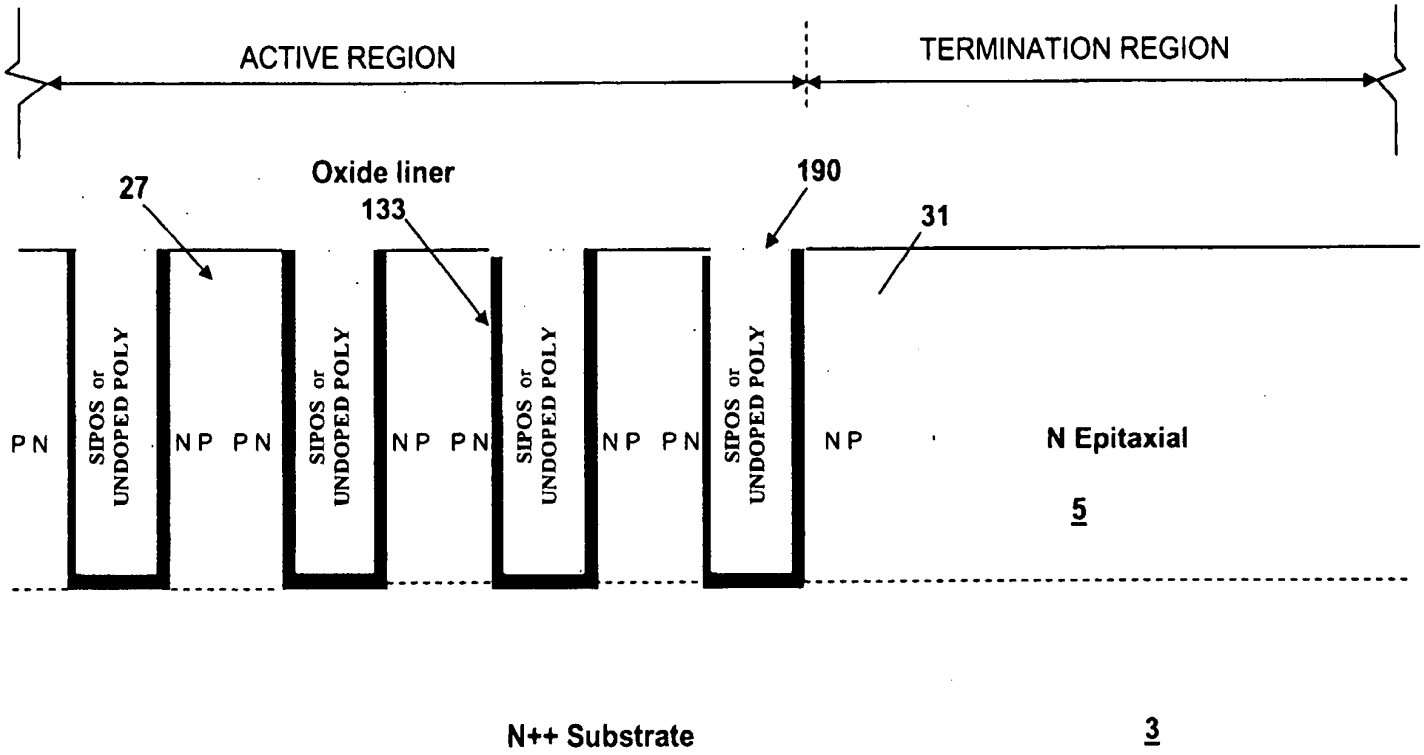
Title: Superjunction Device ... Oxide Lined Trenches
Inventor: Samuel Anderson Customer No.: 570
Express Mail Label No.: EV 553432430 US
Atty. Docket No.: 681443-1US

Fig. 4

Embodiment 1
N-Type Structure

Trench refill with Oxide liner (100 Å to 1 µm)
then refill with undoped poly

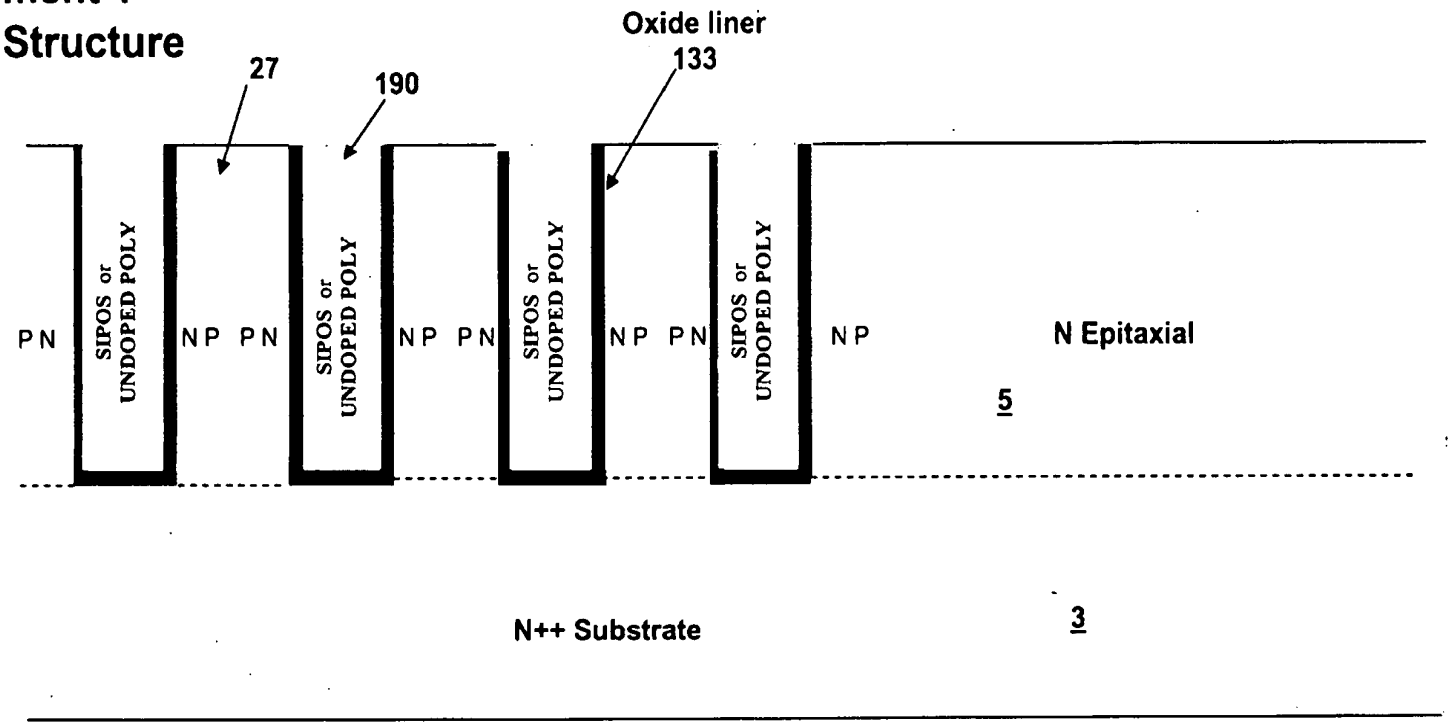
Planarization



Title: Superjunction Device ... Oxide Lined Trenches
Inventor: Samuel Anderson Customer No.: 570
Express Mail Label No.: EV 553432430 US
Atty. Docket No.: 681443-1US

Fig. 5

Embodiment 1
N-Type Structure



Title: Superjunction Device ... Oxide Lined Trenches
Inventor: Samuel Anderson Customer No.: 570
Express Mail Label No.: EV 553432430 US
Atty. Docket No.: 681443-1US

The above structure can be used to made N-MOSFET by adding the following steps :

1) clean the silicon surface
2) gate oxide growth
3) poly gate
4) P-body and guard rings
5) N+ source
6) source metal

The N-MOSFET structure is shown in the next page

Fig. 6

NP-PN Mesa

(Embodiment 1)

N-Type Planar MOS

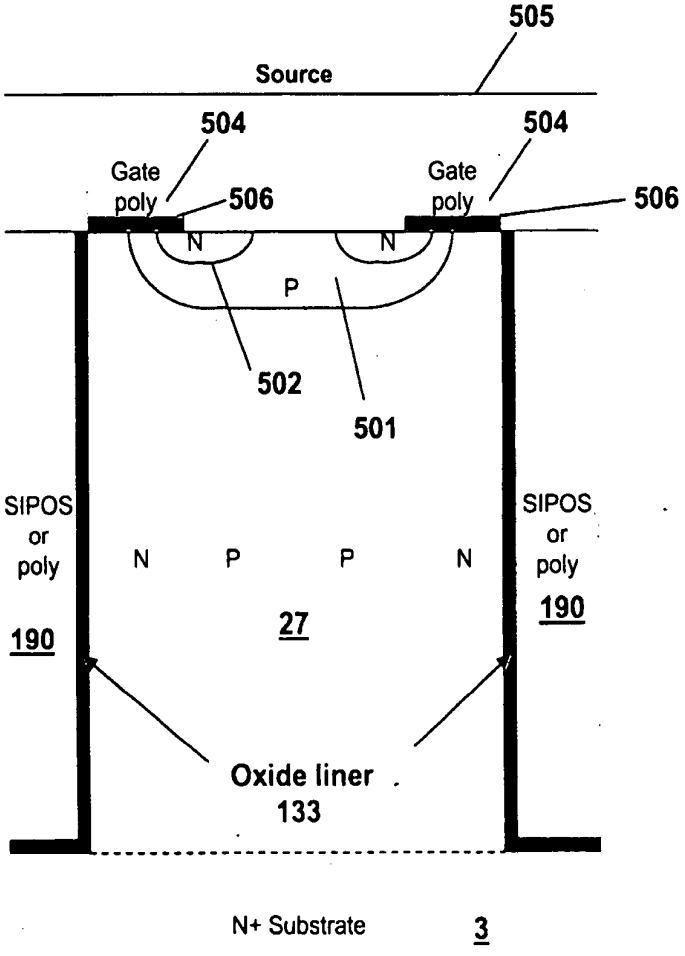


Fig. 7

PN-NP Mesa

(Embodiment 1)

N-Type Planar MOS

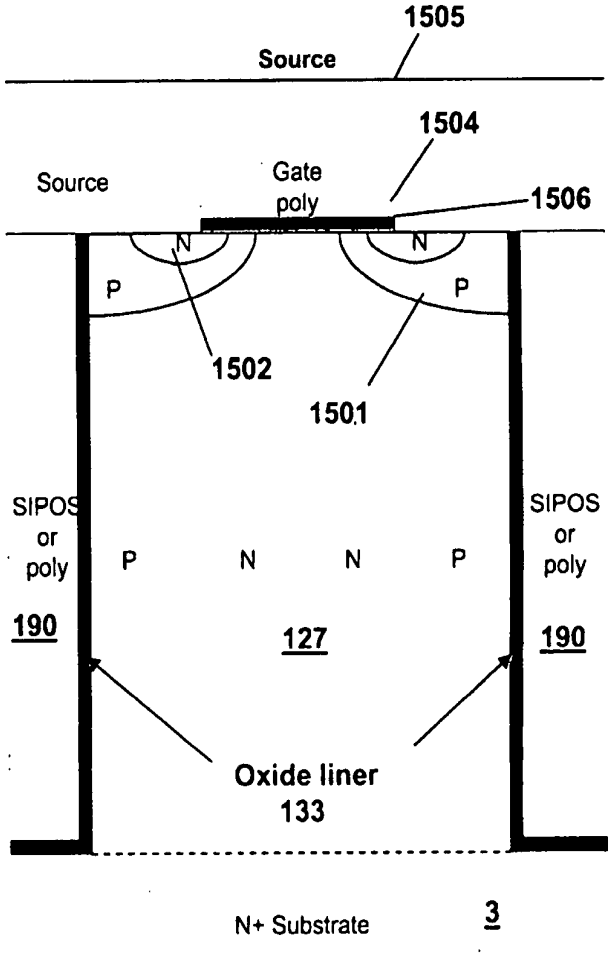


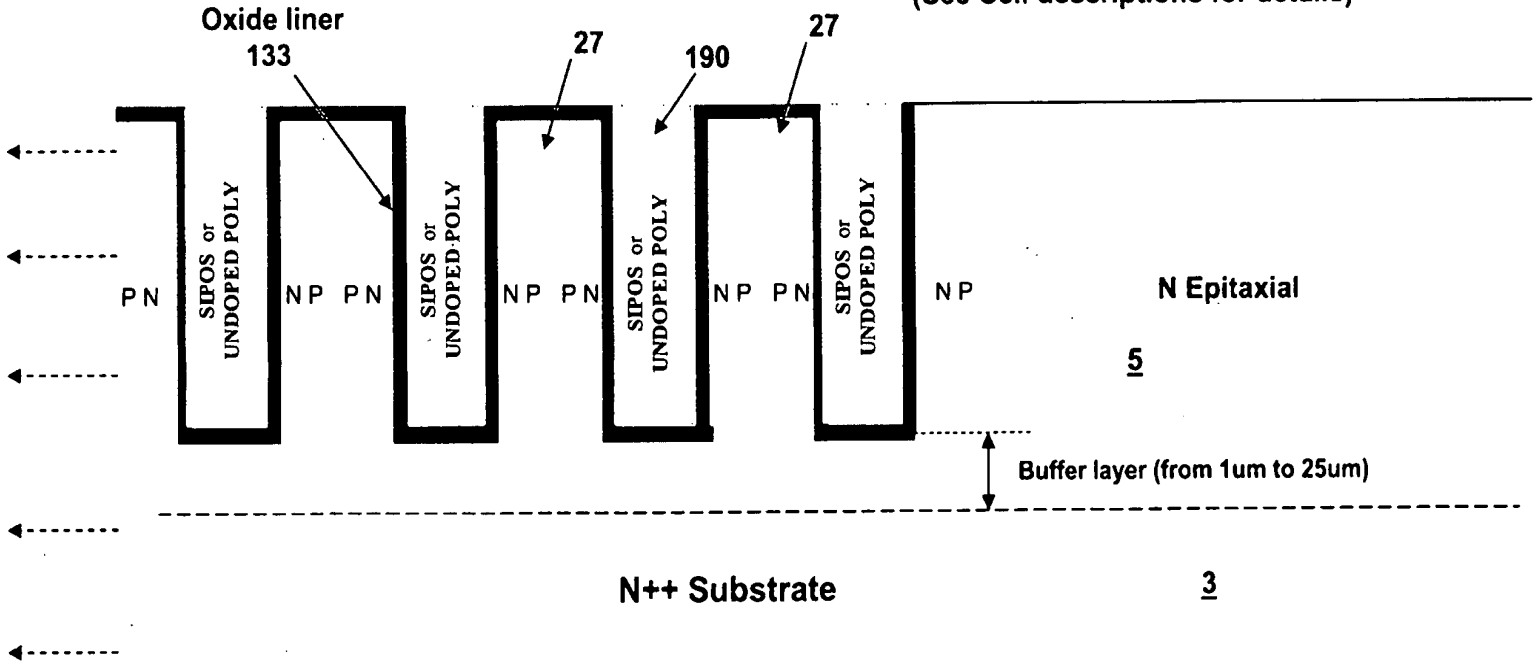
Fig. 8

Title: Superjunction Device ... Oxide Lined Trenches
Inventor: Samuel Anderson Customer No.: 570
Express Mail Label No.: EV 553432430 US
Atty. Docket No.: 681443-1US

Embodiment 2
N-Type Structure

With buffer layer between the
N/P columns and substrate

Trench etch
P implant +4 degree
P implant -4 degree
Diffusion
N implant +4 degree
N implant -4 degree
Diffusion
Trench refill with Oxide liner (100 Å to 10,000 Å)
then refill with undoped poly
P-Body implant and diffusion
(See Cell descriptions for details)



Title: Superjunction Device ... Oxide Lined Trenches
Inventor: Samuel Anderson Customer No.: 570
Express Mail Label No.: EV 553432430 US
Atty. Docket No.: 681443-1US

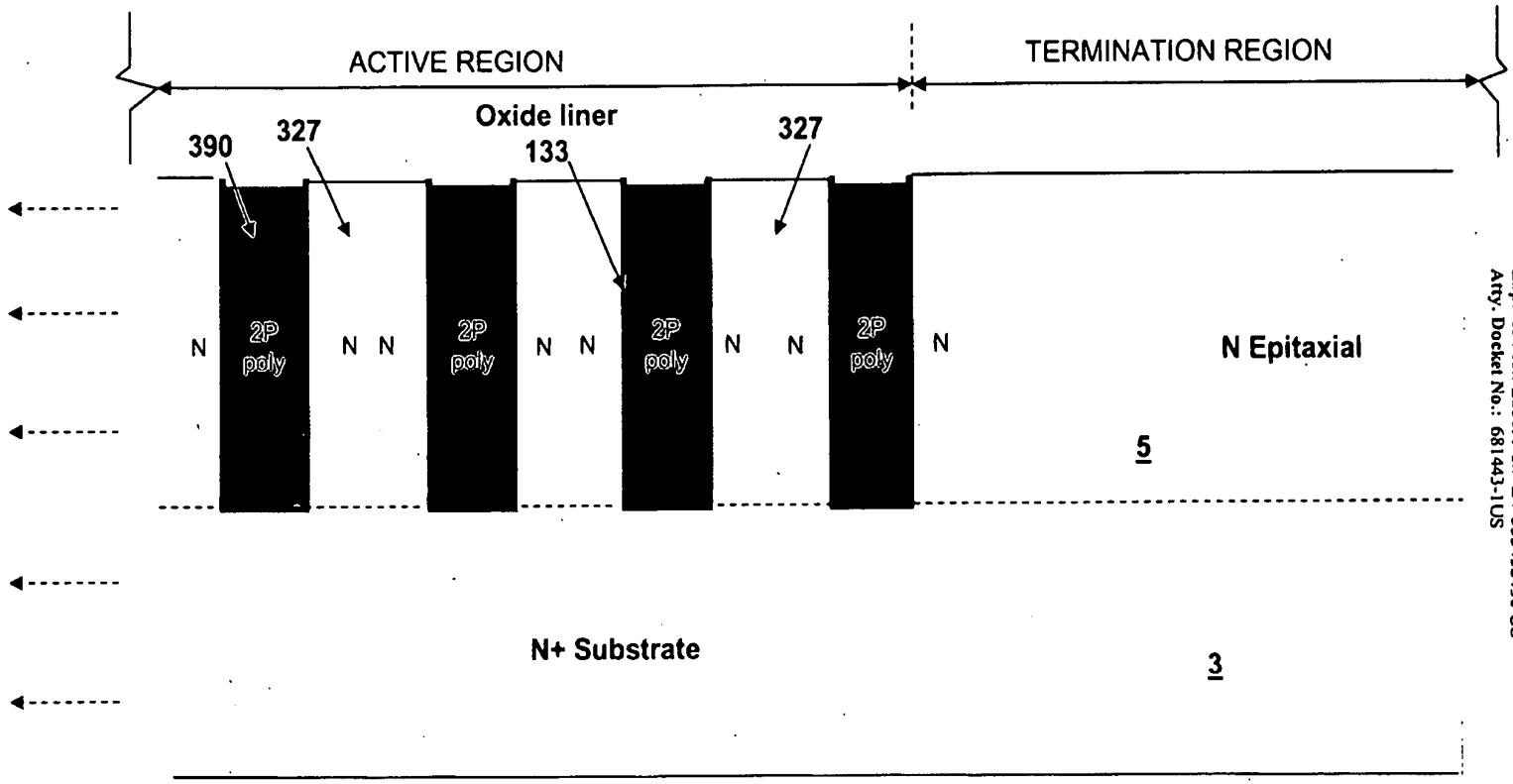
Notes: (1) N_column and P_column can be exchanged
(2) For P Channel device, substrate is P+,
(3) For N Channel device, substrate is N+
(4) The Oxide liner is formed by LPCVD TEOS
(5) the fill can be SIPOS (O2 content from 1% to 99%) or undoped Poly
(6) The method can be used to make N-MOSFET , P-MOSFET and Schottky diode

Fig. 9

Embodiment 3
N-Type Structure

With Oxide liner
between N_Column and P_Column

Trench
N implant +4 degree
N implant - 4 degree
Diffusion
Refill Oxide liner (from 100 Å to 10,000 Å)
Refill Un-doped poly (from 100 Å to 10,000 Å)
P implant +4 degree (or – 4 degree)
Un-doped poly refill
Planarization



Notes: (1) N_column and P_column can be exchanged
(2) For P Channel device, substrate is P+,
(3) For N Channel device, substrate is N+
(4) The Oxide liner is formed by LPCVD TEOS
(5) The method can be used to make N-MOSFET , N-MOSFET and Schottky diode

Fig. 10

Embodiment 3
N-Type Structure

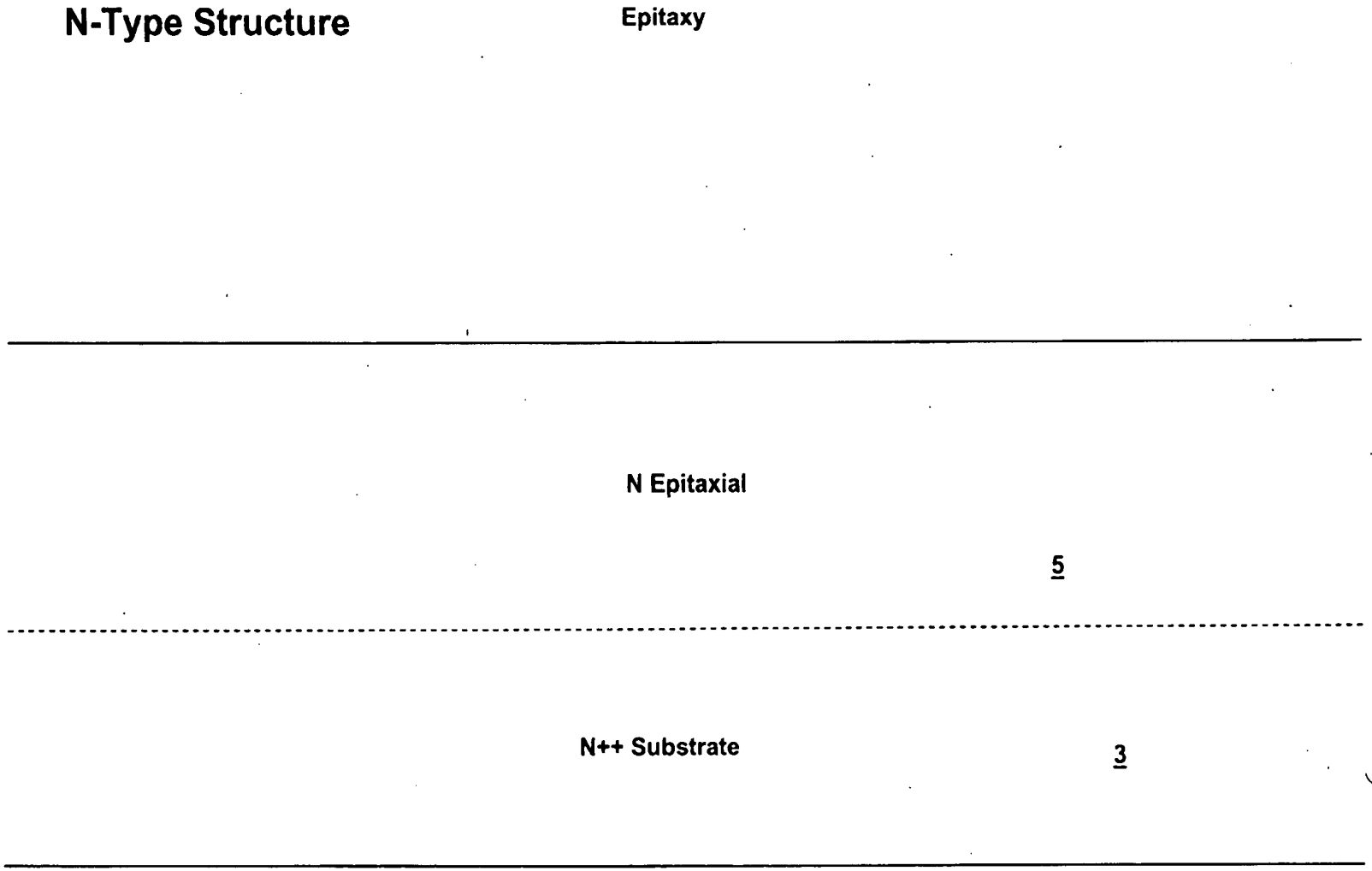


Fig. 11

Title: Superjunction Device ... Oxide Lined Trenches
Inventor: Samuel Anderson Customer No.: 570
Express Mail Label No.: EV 553432430 US
Atty. Docket No.: 681443-1US

Embodiment 3
N-Type Structure

Trench etch
N implant +4 degree
N implant -4 degree
Diffusion

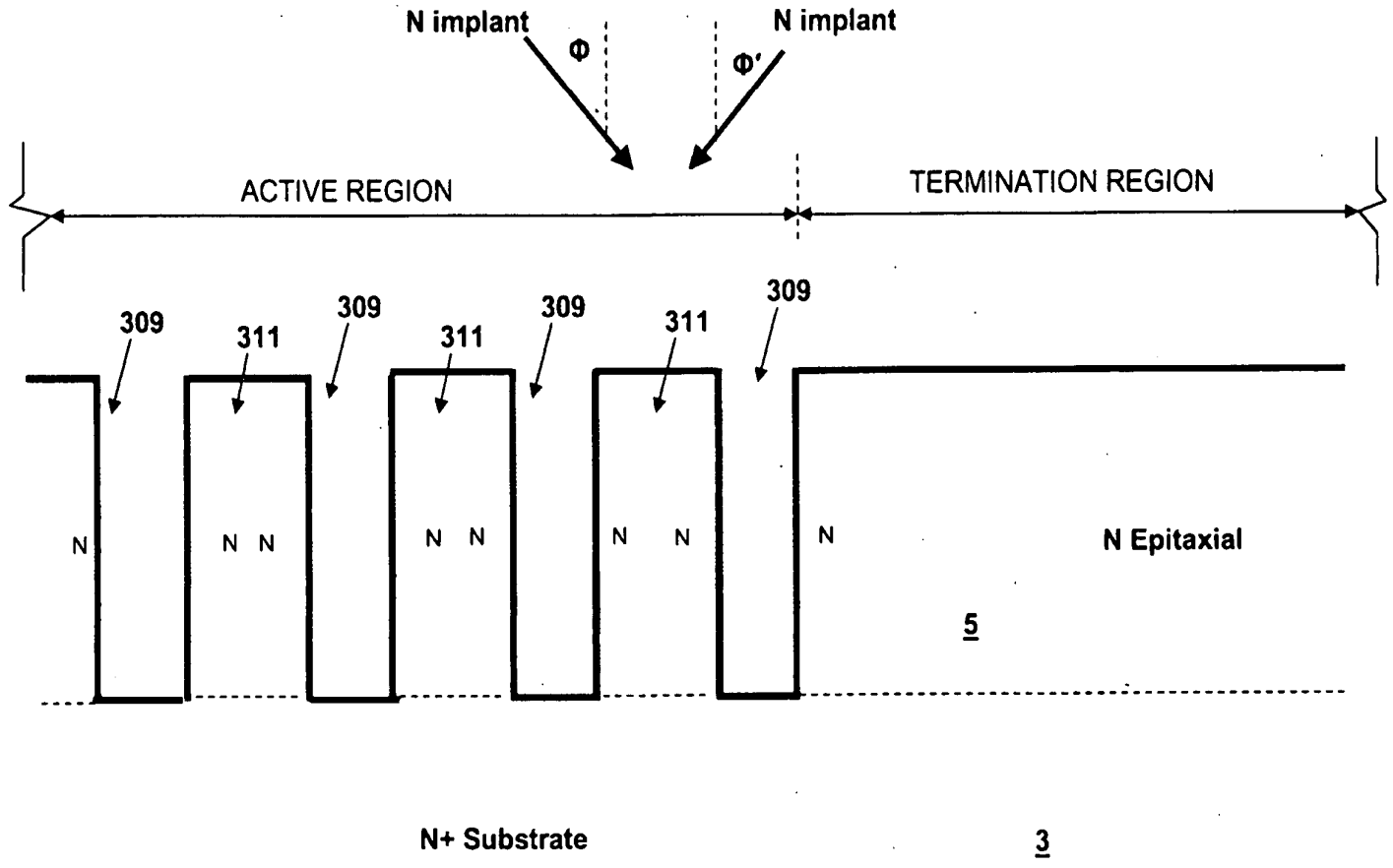


Fig. 12

Embodiment 3
N-Type Structure

Refill with Oxide liner (from 100 Å to 10,000 Å)
Refill with Un-doped poly (from 100 Å to 10,000 Å)
P implant +4 degree (or – 4 degree)

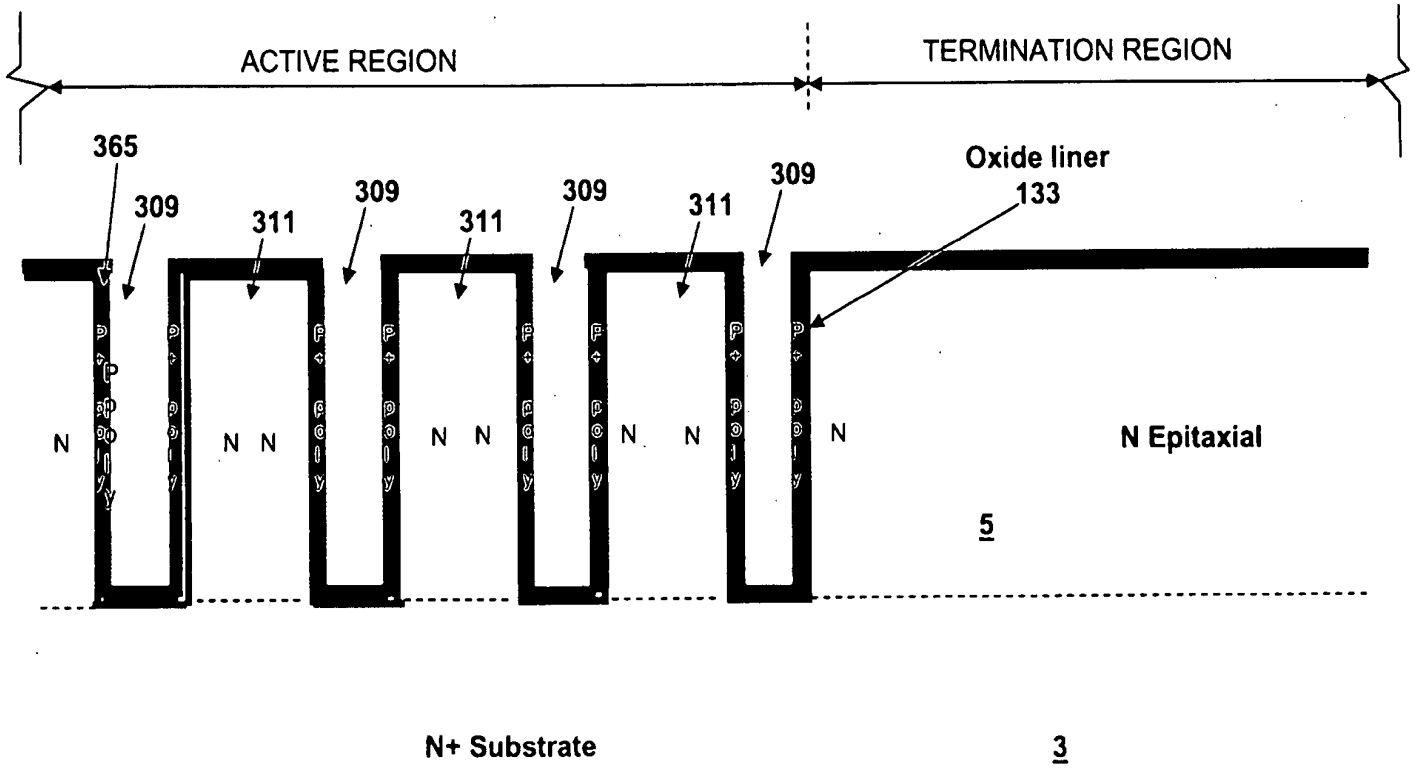


Fig. 13

Embodiment 3
N-Type Structure

Un-doped poly refill planarization

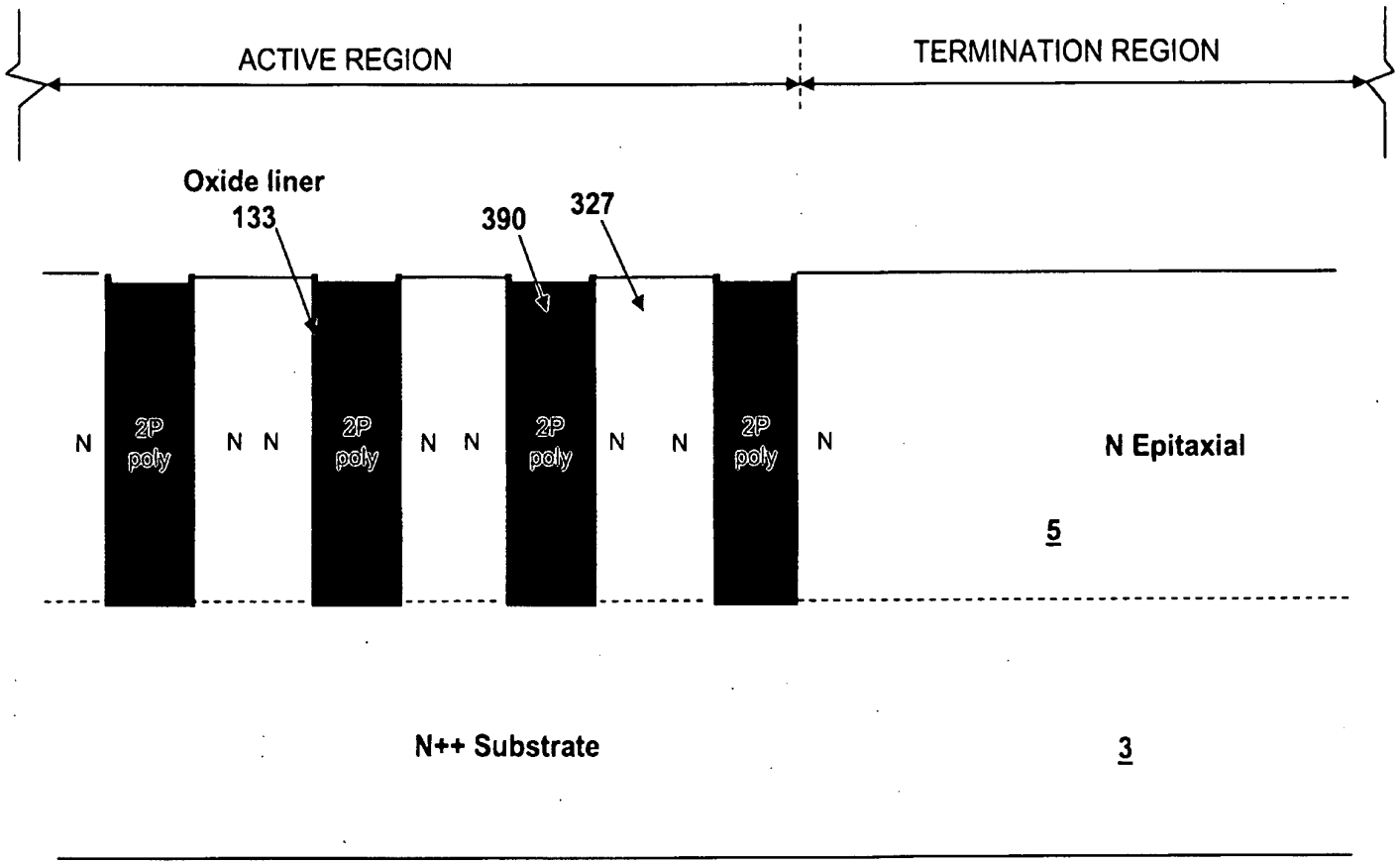
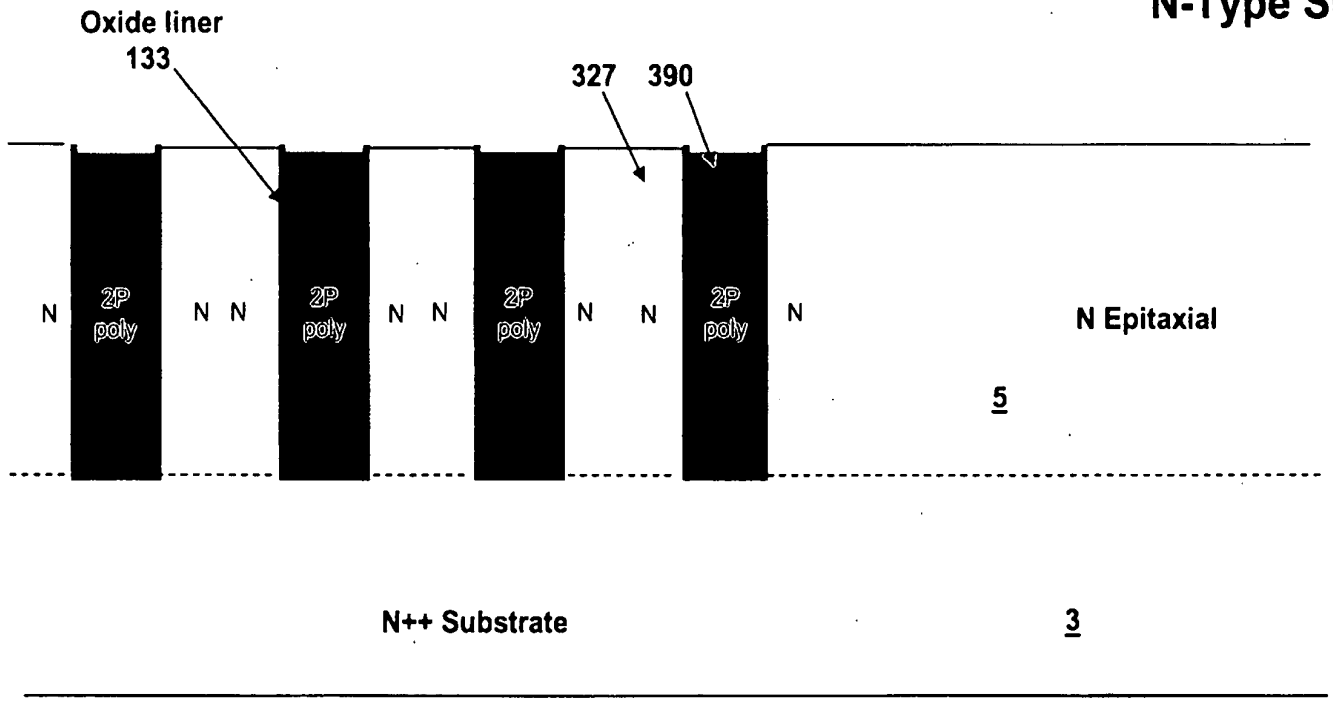


Fig. 14

Embodiment 3
N-Type Structure



The above structure can be used to made N-MOSFET by adding the following steps :

1) clean the silicon surface
2) gate oxide growth
3) poly gate
4) P-body and guard rings
5) N+ source
6) source metal

Fig. 15

An N-MOSFET structure is shown in Fig. 16

Title: Superjunction Device ... Oxide Lined Trenches
Inventor: Samuel Anderson Customer No.: 570
Express Mail Label No.: EV 553432430 US
Atty. Docket No.: 681443-1US

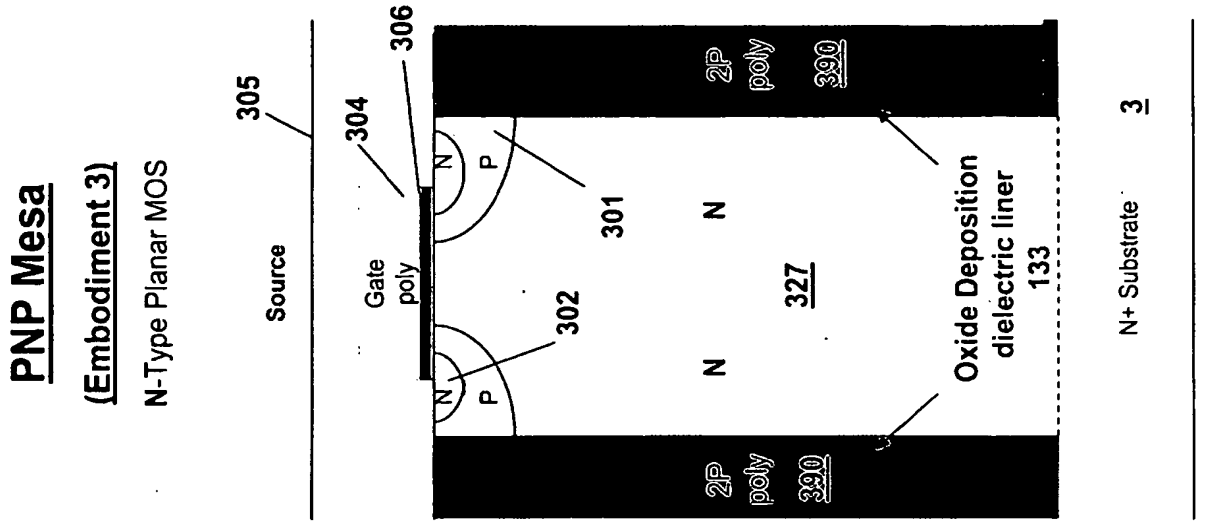
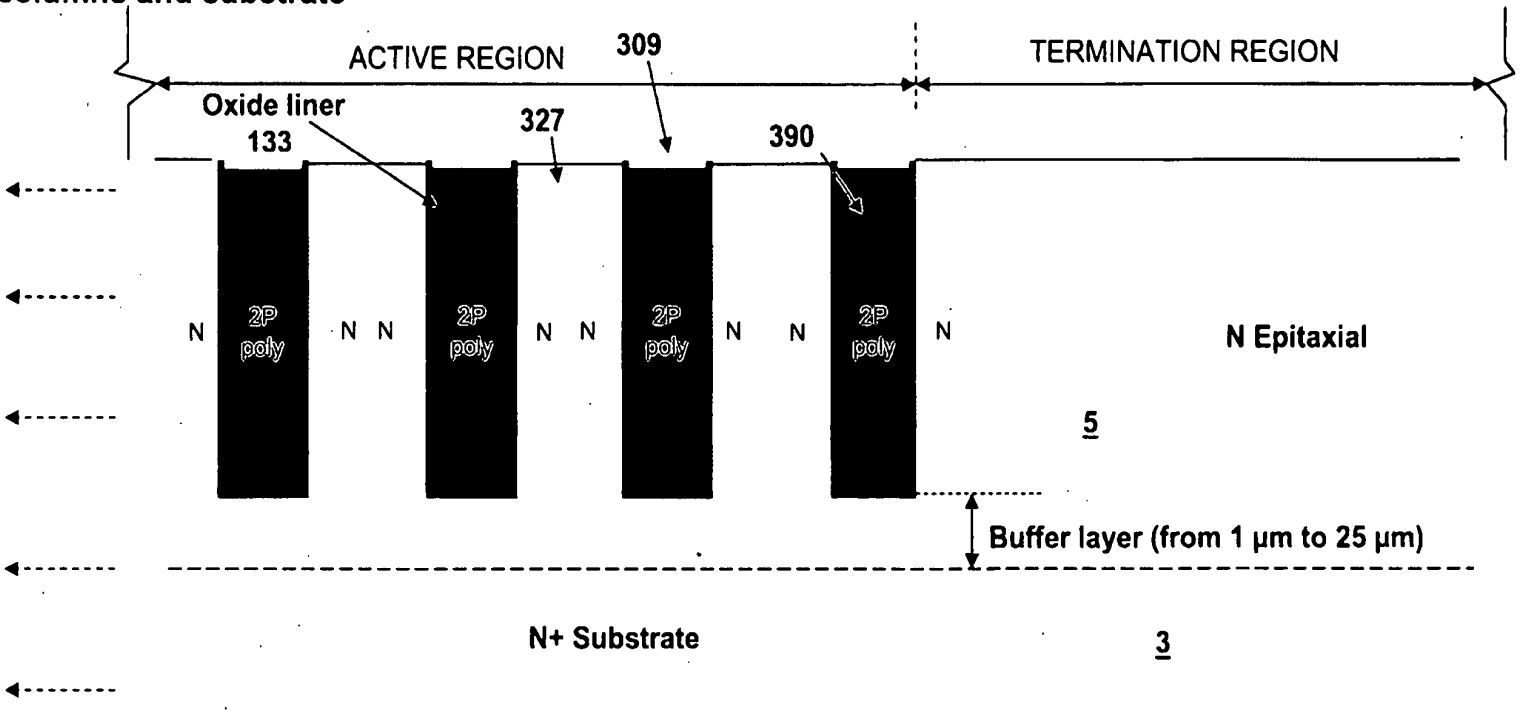


Fig. 16

Embodiment 4
N-Type Structure

With Oxide liner
between N_Column and P_Column
With a buffer layer between the N/P columns and substrate

Trench
N implant +4 degree
N implant - 4 degree
Diffusion
Refill with Oxide liner (from 100 Å to 10,000 Å)
Un-doped poly (from 100 Å to 10,000 Å)
P implant +4 degree (or – 4 degree)
Un-doped poly refill
Planarization



Notes: (1) N_column and P_column can be exchanged
(2) For P Channel device, substrate is P+,
(3) For N Channel device, substrate is N+
(4) The Oxide liner can be SIPOS (O_2 content from 1% to 99%) and Silicon rich nitride etc
(5) The method can be used to make N-MOSFET , N-MOSFET and Schottky diode

Fig. 17